John Cohn Ph.D.

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Education

Ph.D.	**Computer Engineering** **Carnegie Mellon University** *Thesis work in Layout Automation for Analog VLSI* *Published as "Analog Device-Level Layout Automation"* *Kluwer Press 1991*	1988 - 91
BSEE	**Electrical Engineering** **Massachusetts Institute of Technology** *Thesis work in Device Fabrication* *(Includes 1979-1980 at Institut fur Europaische Studiem, Vienna Austria)*	1977 - 81

Professional Positions

Chief Scientist	**MIT-IBM Watson AI Lab** *IBM Fellow - Tech lead for 50 person team doing Neuro-symbolic AI and AI for embedded systems on MIT Campus*	2018 – >
Chief Scientist	**IBM Watson Internet of Things** *IBM Fellow - Technology lead for Worldwide IoT Headquarters Munich Germany*	2015 – 18
Staff Member	**IBM Corporate Technical Strategy** *IBM Fellow - Founding member Corporate SPEED Innovation Team*	2012 – 15
Chief Scientist	**IBM Electronic Design Automation** *IBM Distinguished Engineer / IBM Fellow - Led 400 person design automation team in design tools and methodologies for high speed digital and analog and mixed signal design*	1991 – 12
Ph.D. Student	**Carnegie Mellon University** *Doctoral research in analog/mixed signal layout automation*	1988 – 81
Staff Engineer	**IBM Analog Specials** *Led creation of first commercial analog/mixed signal IC flow*	1981 – 81

Awards and Recognition

IEEE CAS	**IEEE CAS John Choma Education Award** *For successful evangelizing of the essential role of STEM education*	2019
Carnegie Mellon University	**CMU Alumni Distinguished Achievement Award** *For pioneering work in design automation for high speed circuits and for sharing passion for science.*	2014
Webby Award	**for Play! STEM social media campaign** *From IBM and Ogilvy*	2016
Cannes Lions	**Bronze Lion Play! STEM Short** *From IBM and Ogilvy*	2015
VASE	**Elected Vermont Academy of Science and Engineering (VASE)** *Outreach chair 2014-presesent*	2010 -
IBM Corp	**Appointed IBM Fellow** *for contributions to high speed integrated design* *1 of 90 in IBM's more than 200,000 technical employees*	2006 -
	Elected VP of Americas for IBM Academy	2007 – 10
	Named IBM Master Inventor	2005
	Outstanding Technical Achievement – SPAM Circuit Recogniton	2000
	Appointed IBM Distinguished Engineer	1999
	Elected IBM Academy – IBM' top 300 technical leaders	1996
	Outstanding Technical Achievement – IBM Circuit Bench	1995
IEEE	**Named IEEE Fellow** *for contributions to high speed integrated circuit design*	2005 -
	IEEE Division 1 Award *for Service to the Field and Community*	2004

Professional contributions and appointments

UVM	**Named UVM Distinguished Visiting Scholar** College of Engineering, University of Vermont	2020

	Appointed Adjunct Professor of Computer Science *Taught IC design, Computer aided design, Capstone design projects*	1994
MIT	**Led design and build of Satori IBM Supercomputer at MIT** *#4 on Supercomputing Green500, Now being applied to Covid19 research*	2019
	Led IBM's presence at HackMIT	2019 – 18
	Co-founding officer Vermont's Own MIT (VoMIT) alumni club	2013 ->
CMU	**Named to Electrical and Computer Engineering Board of Advisors**	2019
State of VT	**Appointed to VT Task force on Artificial Intelligence by VT Senate**	2018 - 19
	Appointed to VT Task force on Phosphorous by Vt Sec'y of State	2017 - 18
	Appointed to VT State Science Content Committee	1998 -
SRC	**Named BM representative to Semiconductor Research Board (SRC)** *Helped set university research agenda in multi company consortium'* *Contributed to Int'l Technology Roadmap for semiconductors (ITRS)*	1996 – 06 *2001 - 02*
IEEE	**Elected board member in Green Mountain Section of IEEE** *Education Outreach chair*	2012 - 2012 -
	Many conference committees, paper review committees, etc *CICC, DAC, ICCAD, ISCCC, ITC, ISCAS, ISSCC, IEEE Student Conferences*	1991 -
SamStones.org	**Created kids charity SamStones.org** *to support kids love of music, snowboarding, camping ,etc in memory of our son Sam who died in 2006*	2007

Publications

Books and Book Chapters	Osler PJ, Cohn JM, Chinnery D. Design closure. In Handbook of Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology: CRC Press. 2016 Apr 27:295.	2016
	Rutenbar RA, Cohn JM, Lin MP, Baskaya F. Layout Tools for Analog Integrated Circuits and Mixed-Signal Systems-on-Chip: A Survey. In Handbook of Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology (pp. 501-522). CRC Press.	2016
	Stok L, Puri R, Bhattacharya S, Cohn J, Sylvester D, Srivastava A, Kulkarni S. Pushing ASIC performance in a power envelope. In Closing the Power Gap between ASIC & Custom (pp. 323-356). Springer, Boston, MA.	2007

	J Cohn, D Garrod, R Rutenbar, and R Carley, KOAN/ANAGRAM II: New Tools for Device-Level Analog Placement and Routing, In Computer-Aided Design of Analog Integrated Circuits and Systems, Edited R. Rutenbar G. Gielen, B. Antao, John Wiley and Sons.	2006
	R Rutenbar, and J Cohn, *Layout Tools for 'Analog ICs and Mixed-Signal SoCs*, In Computer-Aided Design of Analog Integrated Circuits and Systems, Edited R. Rutenbar, G. Gielen, B. Antao, John Wiley and Sons.	*2006*
	Cohn JM. Technology Challenges for SOC Design. In Winning the SoC Revolution 2003 (pp. 255-296). Springer, Boston, MA.	2003
	Cohn JM, Garrod DJ, Carley R, Rutenbar RA. Analog device-level layout automation. Springer Science & Business Media; 1994 Jan 31. *Widely used reference for analog CAD*	1994
Articles	Li J, Han Song, Gan C, Cohn. Et. al MCUNet: Tiny Deep Learning on IoT Devices. Spotlight paper. NeuRIPS 2020	2020
	J. Meklenburg, M. Specter, M Wentz, A Chandrakasan, J Cohn, R Rivest Et. al, SonicPACT: An Ultrasonic Ranging Method for the Private Automated Contact Tracing (PACT) Protocol, https://arxiv.org/abs/2012.04770	2020
	C Chen, R Panda, R Feris, J Cohn, A Oliva, Q Fan Deep Analysis of CNN-based Spatio-temporal Representations for Action Recognition. https://arxiv.org/abs/2010.11757 ICCV 2021	2020
	Ploennigs J, Cohn J, Stanford-Clark A. The Future of IoT. IEEE Internet of Things Magazine. 2018 Nov 29;1(1):28-33.	2018
	Benson K, Fracchia C, Wang G, Zhu Q, Almomen S, Cohn J, D'arcy L, Hoffman D, Makai M, Stamatakis J, Venkatasubramanian N. SCALE: Safe community awareness and alerting leveraging the internet of things. IEEE Communications Magazine. 2015 Dec 17;53(12):27-34.	2015
	Li C, Wang D, Boenke M, Letavic T, Cohn J. An integrated zigbee transmitter and DC-DC converter on 0.18 µm HV RF CMOS technology. In2013 IEEE 10th International Conference on ASIC 2013 Oct 28 (pp. 1-4). IEEE.	2013
	Cohn J. Engineering paradise: Inspiring the next generation to build a smarter planet. In2010 IEEE International Test Conference 2010 Nov 2 (pp. 13-14). IEEE.	2010
	J. L. Martin, H. Varilly, J. Cohn and G. R. Wightwick, Technologies for a Smarter Planet in IBM Journal of Research	2010

and Development, vol. 54, no. 4, pp. 1-2, July-Aug. 2010.

Field RM, Lary J, Cohn J, Paninski L, Shepard KL. A low-noise, single-photon avalanche diode in standard 0.13 μ m complementary metal-oxide-semiconductor process. Applied Physics Letters. 2010 Nov 22 2010

Cohn J. Kids today! Engineers tomorrow?. In 2009 IEEE International Solid-State Circuits Conference-Digest of Technical Papers 2009 Feb 8 (pp. 29-35). IEEE. 2009

“Design and CAD Challenges for Leading-Edge Multimedia Designs”, A Kahng, I Chayut , J Cohn , T Hattori, JT Kong , P Paulin, Tobias, IEEE Design & Test of Computers Year: 2007 | Volume: 24, Issue: 1 2007

Cohn J, Kong JT, Malachowsky C, Tobias R. Design challenges for next-generation multimedia, game and entertainment platforms. In Proceedings of the 43rd annual Design Automation Conference 2006 Jul 24 (pp. 459-459). 2006

"What is the next implementation fabric?," J. Cohn et.al IEEE Design & Test of Computers, vol. 20, no. 6, pp. 86-95, Nov.-Dec. 2003. 2003

Stok L, Cohn J. There is life left in ASICs. In Proceedings of the 2003 international symposium on Physical design 2003 Apr 6 (pp. 48-50). 2003

Puri R, Stok L, Cohn J, Kung D, Pan D, Sylvester D, Srivastava A, Kulkarni S. Pushing ASIC performance in a power envelope. In Proceedings of the 40th annual Design Automation Conference 2003 Jun 2 (pp. 788-793). 2003

Lackey DE, Zuchowski PS, Bednar TR, Stout DW, Gould SW, Cohn JM. Managing power and performance for system-on-chip designs using voltage islands. In Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design 2002 Nov 10 (pp. 195-202). 2002

Bergamaschi RA, Cohn J. The A to Z of SoCs. In Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design 2002 Nov 10 (pp. 790-798). 2002

Rutenbar RA, Cohn JM. Layout tools for analog ICs and mixed-signal SoCs: a survey. In Proceedings of the 2000 international symposium on Physical design 2000 May 1 (pp. 76-83). 2000

EDIF in IBM, Proceedings of EDIF World, Portland ME 1992

J. Cohn, Placement of Analog Circuits in KOAN Ph.D. dissertation, Carnegie Mellon University. Available as an SRC Tech. Doc — 1991

Cohn JM, Garrod DJ, Rutenbar RA, Carley LR. KOAN/ANAGRAM II: New tools for device-level analog placement and routing. IEEE Journal of Solid-State Circuits. 1991, Mar;26(3):330-42. — 1991

Cohn JM, Garrod DJ, Rutenbar RA, Carley LR. Techniques for simultaneous placement and routing of custom analog cells in KOAN/ANAGRAM II. In1991 IEEE International Conference on Computer-Aided Design Digest of Technical Papers 1991 Nov 11 (pp. 394-397). IEEE. — 1991

Cohn JM, Garrod DJ, Rutenbar RA, Carley LR. New algorithms for placement and routing of custom analog cells in ACACIA. In IEEE Proceedings of the Custom Integrated Circuits Conference 1990 May 13 (pp. 27-6). IEEE. — 1990

J. Cohn, D. Garrod, R. A. Rutenbar and L. R. Carley, KOAN/ANAGRAM II: Flexible Algorithms for Layout of Custom Analog Cells, Extended Abstract Volume, Semiconductor Research Corporation TECHCON'90, October, 1990 — 1990

Talks and Tutorials

Many worldwide talks, tutorials, panels and keynotes including the following sampling:

Think Digital Summit Israel - "What's Next: Atoms, Neurons and Qubits" 2020
28 November 2020.

C2 Montréal 2020: Beyond Boundaries "Workshop: Inventors like You!" 2020
Picked as conference highlight. October 28, 2020

Mass Open Cloud Workshop, "Big Blue meets Mass Green" 2020
March 3, 2020

Think Singapore - "The Future of Computing" 2019
Marina Bay Sands Expo & Convention Centre
Singapore | 14 August 2019.

SXSW Austin "Prioritizing Play in An Automated Age" 2019
IEEE Tech for Humanity Series, SXSW Austin Mar 9

Think Madrid - AI: Bringing the Future Closer 2018
Área de Exposición, Madrid, Span Nov 2018

Think Sydney 'Digital Disruption and the Internet of Things 2018
Where Technology meets Humanity Sydney Australia, May

TED Summit, Unleash Your Inner Mad Scientist, workshop 2016
June 26–30, 2016 · Banff, Canada

IBM Interconnect "Serious Play- Serious Play: An Engineer's 2016
Perspective on Fun and Passion at Work" Las Vegas, NV

Keynote Speaker ACM World Programming Finals. 2015
Marrakesh Morocco

Keynote at IEEE Transmitter Series 2015
Consumer Electronics Show (CES)

Career Panelist Society of Woman Engineers Annual Meeting 2015
Nashville , TN

"The Importance of Play" TEDx Delft 2013
Delft Netherlands

Invited Plenary Keynote "Kids Today, Engineers Tomorrow ? " 2009
IEEE International Solid State Circuits Conference (ISSCC), San Francisco, Feb 2009

Invited Keynote "Kids today*" IEEE International Symposium on* *2008*
Circuits and Systems (ISCAS), Seattle, May 2008

Keynote Speaker ACM World Programming Finals. 2005
Shanghai , China

Design Automation Conference Panel"Place Your Bets" 2003
Won audience choice on my positions

Invited tutorial "AtoZ's of SoC's" 2002
International Conf on Computer Aided Design (ICCAD02)

Invited Panel: CAD for CAD's Sake 2002
International Conf on Computer Aided Design (ICCAD02)

Brickwalls and Breakthroughs 2001
CANDE Workshop Yellowstone Lodge Sept 2001 (!)

Invited Panel Moderator "Who has nanometer design under control?" 2001
Design Automation Conference (DAC2001)

Invited Panel Moderator "Design on the Bleeding Edge" 2000
Design Automation Conference (DAC2000)

Computer-Aided Design of VLSI Interconnect, Invited Tutorial 1997
International Conf on Computer Aided Design (ICCAD97)
Highest rated tutorial of the conference

Computer-Aided Design of VLSI Interconnect, Invited Tutorial 1996

International Conf on Computer Aided Design (ICCAD96)
Highest rated tutorial of the conference

Computer-Aided Design of VLSI Interconnect, Invited Tutorial 1994
International Conf on Computer Aided Design (ICCAD94)

Computer-Aided Design of VLSI Interconnect, Invited Tutorial 1993
International Conf on Computer Aided Design (ICCAD93)

STEM Promotion

Live Shows

29 years of tye-dyed 'Mad Science' STEM electricity shows. 1991 -
Demonstrating micro-volts to megavolts in fun, participatory way. In classrooms, school auditoriums, scout groups, camps, universities. Special need groups, inner cities, conferences. The Smithsonian Museum, Shanghai Science Museum, Ny Hall of Science, Montreal Science Museum, Disney, all over the world.> 60,000 students wowed !

Science Talks / Demos

Hundreds of fun and provocative STEM-themed Science talks 1991 -
Talks/demos in schools, Universities, clubs, camps, museums, conferences, Festivals in more than 40 countries around the world .
Talks include:

- ***The Importance of Play / Serious Play*** *– the importance of play in inventing*
- ***Do try this at home !*** *– The importance of hands-on experimentation*
- ***The Joy of making things*** *- about the existential joy of being an engineer*
- ***Lessons from 'The Colony'*** *– lessons from the Discovery STEM Show 'The Colony'*
- ***Kids these days*** *– about the joys of STEM Careers*
- ***High Tension: the life and times of Nikola Tesla*** *– all about the famous Inventor*
- ***Inventors like you*** *– Showing the diversity of Inventors through the ages.*

Tesla Science Center

Named to advisory board of the Tesla Science Center Shoreham NY 2020
New museum at the site of Nikola Tesla's only surviving laboratory

VASE

Created VT Academy of Science and Engineering Grants Programs 2014
Hands-on Science and Tech Grants for extracurricular science
VASE Small Equipment Grants for classroom science
~17K$ in annual grants to VT Teachers and STEM Students

Discovery Channel

Co-starred in Discovery Channel hit STEM reality show "The Colony" 2009
Played to worldwide audiences and replayed for many years
Served as science advisor to The Colony Season II

Makerspaces

Co-founder of Vermont Makers linking technologists and artists
Founder of Watson IoT Makerspace, Munich, Germany 2016
Founding board member of Generator VT's largest Makerspace. *2013*
Founder of Vermont FabLab at University of Vermont 2012

ECHO Museum

Elected Board of ECHO Science Museum, Burlington, VT 2011 – 17

	Vermont's largest hands on science museum	
Governors Institute	**Annual talks in Vermont Governors Institute of Vermont (GIV) camps** *Engineering Summer Camp* *Design, Media and Games Summer Camp*	2007 -
FIRST Robotics	**Leading First Tech Challenge statewide expansion Program** Received $40K FIRST STEM Equity Grant to spread FISRT Tech Challenge across Vermont Co-lead introduction of FIRST Robotics to the State of Vermont	2020 2020 2013 -
National Engineers Week	**Co-led IBM's Technical Education Outreach (TEO) group** engaging IBMers worldwide in National Engineering Week (NEW) and similar Programs. *Performed at NEW Annual event at Smithsonian*	1995 - 06
Social Media	***Promoting love of STEM careers using social networking tools***	
	Innovation through Play https://youtu.be/AnjFgSvj3vU *Done with Ogilvy talking about how play leads to innovation*	2015
	The Importance of Play https://youtu.be/I-NT1-BdOvI *Popular video of TEDx Delft presentation*	2013
	"Engineering Paradise" https://youtu.be/Y0DxmthvkKU *(really bad ☺) STEM based rap song..*	2010
	Johns Maker projects used to show others the fun of STEM *http://johncohn.org/base/geek-stuff-2/nerd-cred/*	1991 -
	Mainstream coverage in popular media outlets *e.g* : *HuffPost, CNN, CBS, Discovery Channel, EETimes, C2 Magazine, , USAToday* , Frankfurter Allgemine, El Pais , etc	1991 -

Patents

>120 worldwide patents issued n circuit design, design automation, internet of things and AI including:

US10372767 sensor based context augmentation of search queries

US10275519 sensor based context augmentation of search queries

US10257270 autonomous decentralized peer-to-peer telemetry

US10254725 utilizing automated lighting system to determine occupancy

US10079881 device self-servicing in an autonomous decentralized peer-to-peer environment

US9332362 acoustic diagnosis and correction system

US9172718 endpoint load rebalancing controller

US9160763 endpoint load rebalancing controller

US8964995 acoustic diagnosis and correction system

US8423328 method of distributing a random variable using statistically correct spatial interpolation ...

US8299609 product chips and die with a feature pattern that contains information relating to the product chip

US8230378 method for ic wiring yield optimization, including wire widening during and after routing

US8219943 physical design system and method

US8187897 fabricating product chips and die with feature pattern that contains information relating to the product chip

US7961932 method and apparatus for manufacturing diamond shaped chips

US7895545 methods for designing a product chip a priori for design subsetting, feature analysis, and yield learning

US7669170 circuit layout methodology using via shape process

US7669159 ic tiling pattern method, ic so formed and analysis method

US7657859 a method for ic wiring yield optimization, including wire widening during and after routing

US7644327 system and method of providing error detection and correction capability in an integrated circuit using redundant logic cells of an embedded fpga

US7620931 method of adding fabrication monitors to integrated circuit chips

US7558999 learning based logic diagnosis

US7536664 physical design system and method

US7503021 integrated circuit diagnosing method, system and program product

US7469395 wiring optimizations for power

US7373567 a system and method of providing error detection and correction capability in an integrated circuit using redundant logic cells of an embedded fpga

US7346875 wiring optimizations for power

US7323278 method of adding fabrication monitors to integrated circuit chips

US7308669 the use of redunant routes to increase the yield and reliability of a vlsi layout

US7289659 method and apparatus for manufacturing diamond shaped chips

US7285860 method and structure for defect monitoring of semiconductor devices using power bus wiring grids

US7240322 method of adding fabrication monitors to integrated circuit chips

US7239167 utilizing clock shields as defect monitor

US7222248 a method of switching voltage islands in integrated circuits when a grid voltage at a reference location is within a specified range

US7194706 designing scan chains with specific parameter sensitivities to identify process defects

US7188322 circuit layout methodology using a shape processing application

US7135907 clock signal distribution utilizing differential sinusoidal signal pair

US7107469 power down processing islands

US7095063 multiple supply gate array backfill structure

US7093213 method for designing an integrated circuit defect monitor

US7089514defect diagnosis for semiconductor integrated circuits

US7088124 Utilizing clock shields as defect monitor

US7078248 Method and structure for defect monitoring of semiconductor devices using power bus wiring grids

US7071757 Clock signal distribution utilizing differential sinusoidal signal pair

US7005874 Utilizing clock shields as defect monitor

US6998866 Circuit and method for monitoring defects

US6985004 Wiring optimization for power

US6948146 Simplified tiling pattern method

US6924661 Power switch circuit sizing technique

US6832361 System and method for analyzing power distribution using static timing analysis

US6825711 Power reduction by stage in integrated circuit

US6792582 Concurrent logical and physical construction of voltage islands for mixed supply voltage designs

US6751744 Method of integrated circuit design checking using progressive I ndividual network analysis

US6711719 Method and apparatus for reducing power consumption in VLSI circuit

US6687883 System and method for inserting leakage reduction control in logic circuits

US6651230 Method for reducing design effect of wearout mechanisms on signal skew in integrated circuit design

US6574779 Hierarchical layout method for integrated circuits

US6523159 Method for adding decoupling capacitance during integrated circuit

US6523154 Method for supply voltage drop analysis during placement phase of chip

US6490708 Method of integrated circuit design by selection of noise tolerant

US6479974 Stacked voltage rails for low-voltage DC

US6473881 Pattern-matching for transistor level netlists

US6430733 Contextual based groundrule compensation method of mask data set

US6429469 Optical Proximity Correction Structures Having Decoupling Capacitors

US6189132 Design rule correction system and method

US5757657 Adaptive incremental placement of circuits on VLSI chip

US5745735 Localized simulated annealing

US5535134 Object placement aid
J. Cohn , L Heng - describes the 'minimum perturbation compaction algorithm behind IBM's custom layout migration tools. Estimated to have saved >300$M in manual design